In the Specification

Please amend the specification of this application as follows:

Page 1, before the line 1 insert:

--This is a divisional of U.S. Patent Application Serial No. 09/397,540, now U.S. Patent No. 6,693,719. This application claims priority under 35 U.S.C. 119(e)(1) to U.S. Provisional Application No. 60/100,657 filed September 16, 1998.--

Rewrite the paragraph at page 5, line 29 to page 6, line 13 as follows:

--In the network printer system of Figure 1 ~~Multiprocessor~~ multiprocessor integrated circuit 100 communicates with print buffer memory 5 for specification of a printable image via a pixel map. Multiprocessor integrated circuit 100 controls the image data stored in print buffer memory 5 via the network printer system bus 2. Data corresponding to this image is recalled from print buffer memory 5 and supplied to print engine 6. Print engine 6 provides the mechanism that places color dots on the printed page. Print engine 6 is further responsive to control signals from multiprocessor integrated circuit 100 for paper and print head control. Multiprocessor integrated circuit 100 determines and controls where print information is stored in print buffer memory 5. Subsequently, during readout from print buffer memory 5, multiprocessor integrated circuit 100 determines the readout sequence from print buffer memory 5, the addresses to be accessed, and control information needed to produce the desired printed image by print engine 6.--

Rewrite the paragraph at page 8, lines 1 to 25 as follows:

--Multiprocessor integrated circuit 100 is constructed to provide a high rate of data transfer between processors and memory using plural independent parallel data transfers. Crossbar 50 enables

these data transfers. Each digital image/graphics processor 71, 72, 73 and 74 has three memory ports that may operate simultaneously each cycle. An instruction port (I) may fetch 64 bit ~~data~~ instruction words from the corresponding instruction cache. A local data port (L) may read a 32 bit data word from or write a 32 bit data word into the data memories or the parameter memory corresponding to that digital image/graphics processor. A global data port (G) may read a 32 bit data word from or write a 32 bit data word into any of the data memories or the parameter memories ~~or~~ of random access memory 20. Master ~~Processor~~ processor 60 includes two memory ports. An instruction port (I) may fetch a 32 bit instruction word from either of the instruction caches 11 and 12. A data port (C) may read a 32 bit data word from or write a 32 bit data word into data caches 13 or 14, parameter memory 15 of random access memory 10 or any of the data memories, the parameter memories or random access memory 20. Transfer controller 80 can access any of the sections of random access memory 10 or 20 via data port (C). Thus fifteen parallel memory accesses may be requested at any single memory cycle. Random access memories 10 and 20 are divided into 25 memories in order to support so many parallel accesses.--

Rewrite the paragraph at page 12, lines 13 to 27 as follows:

--Frame controller 90 is the interface between multiprocessor integrated circuit 100 and external image capture and display systems. Frame controller 90 provides control over capture and display devices, and manages the movement of data between these devices and memory automatically. To this end, frame controller 90 provides simultaneous control over two independent image systems. These would typically include a first image system for image capture and a second image system for image display, although the application of frame controller 90 is controlled by the user. These image systems would ordinarily include independent frame memories

used for either frame grabber or frame buffer storage. Frame ~~controlled~~ controller 90 preferably operates to control video dynamic random access memory (VRAM) through refresh and shift register control.--

Rewrite the paragraph at page 13, line 30 to page 14, line 29 as follows:

--Figure 3 illustrates an overview of exemplary digital image/graphics processor 71, which is virtually identical to digital image/graphics processors 72, 73 and 74. Digital image/graphics processor 71 includes: data unit 110; address unit 120; and program flow control unit 130. Data unit 110 performs the logical or arithmetic data operations. Data unit 110 includes eight data registers D7-D0, a status register 210 and a multiple flags register 211. Address unit 120 controls generation of load/store addresses for the local data port and the global data port. As will be further described below, address unit 120 includes two virtually identical addressing units, one for local addressing and one for global addressing. Each of these addressing units includes an all "0" read only register enabling absolute addressing in a relative address mode, a stack pointer, five address registers and three index registers. The addressing units share a global bit multiplex control register used when forming a merging address from both address units. Program flow control unit 130 controls the program flow for the digital image/graphics processor 71 including generation of addresses for instruction fetch via the instruction port. Program flow control unit 130 includes; a program counter PC ~~701~~; an instruction pointer-address stage IRA ~~702~~ that holds the address of the instruction currently in the address pipeline stage; an instruction pointer-execute stage IRE ~~703~~ that holds the address of the instruction currently in the execute pipeline stage; an instruction pointer-return from subroutine IPRS ~~704~~ holding the

address for returns from subroutines; a set of registers controlling zero overhead loops; four cache tag registers TAG3-TAG0 ~~collectively called 708~~ that hold the most significant bits of four blocks of instruction words in the corresponding instruction cache memory.--

Rewrite the paragraph at page 18, lines 12 to 25 as follows:

--Global port destination data bus Gdst 107 carries 32 bit destination data of a global bus data transfer. The destination is any register of digital image/graphics processor 71. Buffer 147 in global port 145 sources the data of global port destination data bus Gdst 107. Buffer 147 performs any needed data extraction and sign extension operations. This buffer ~~115~~ 147 operates if the data source is memory, and a load is thus being performed. The arithmetic logic unit result serves as an alternative data source for global port destination data bus Gdst 107. This allows any register of digital image/graphics processor 71 to be the destination of an arithmetic logic unit operation. A global bus temporary holding register GTD 108 is also connected to global port destination data bus Gdst 107.--

Rewrite the paragraph at page 19, lines 15 to 28 as follows:

--Program flow control unit 130 receives the instruction words fetched from instruction cache memory 21 via instruction bus 132. This fetched instruction word is advantageously stored in two 64 bit instruction registers designated instruction register-address stage IRA ~~751~~ and instruction register-execute stage IRE ~~752~~. Each of the instruction registers IRA and IRE have their contents decoded and distributed. Digital image/graphics processor 71 includes opcode bus 133 that carries decoded or partially decoded instruction contents to data unit 110 and address unit 120. As will be later described, an instruction word may include a 32 bit, a 15 bit or a 3 bit immediate field. Program flow control unit 130 routes such an

immediate field to global port source data bus Gsrc 105 for supply to its destination.--

Rewrite the paragraph at page 20, line 12 to page 21, line 9 as follows:

--Figure 5 shows a simplified diagram of master processor 60. Major blocks of master processor 60 are: a floating point unit (FPU) 201; a register file (RF) 202; a register scoreboard (SB) 203 that ensures results of floating point operations and memory loads are available before they are used as sources and arbitrates between data cache and floating point unit 201 for access to their shared write port to register file 202; a data cache controller 204 which also handles the interface to the on-chip memory via the crossbar and to external memory via transfer processor 80; a barrel shifter (BS) 205 that performs shift instructions; compare to zero logic 206; left most one/right most one detection logic (LMO/RMO) 207; integer arithmetic logic unit (ALU) 208 used for add, subtract and logical operations and to compute branch target address during relative branches; interrupt pending register (INTPEN) 209 that receives master processor interrupt signals; interrupt enable register (IE) ~~210~~ 220 that selectively enables or disables interrupts; program counter register (PC) ~~211~~ 221 holds the address of the instruction to be fetched; program counter incrementer (INC) 212 that increments program counter ~~211~~ 221 to point to the next instruction, with the incremented value can also be routed to the register file as a "return" or "link" address; instruction decode logic (DECODE) 213 that decodes instruction and supplies control signals to the operating units; instruction register (IR) 214 that holds the address of the instruction being executed; immediate register (IMM) 215 that stores any instruction immediate data; and the instruction cache controller (ICACHE) 216, ~~,~~ that provides

instructions to be executed, interfaces to transfer processor 80 for cache fills.--

Rewrite the paragraph at page 21, lines 10 to 26 as follows:

--Figure 6 shows the basic pipeline used in master processor 60. Master processor 60 has a three stage pipeline including fetch, execute and memory stages. Figure 6 shows how three instructions through the pipeline. During the fetch stage of the pipeline program counter ~~210~~ 221 is used to address the instruction cache and read a 32 bit instruction. During the execute stage the instruction is decoded, the source operands read from the register file, the operation performed, and a result written back to the register file. The memory stage is only present for load and store operations. The address calculated during the execute stage is used to address the data cache and the data are read or written. If a miss occurs on the instruction cache, the fetch and execute pipelines are stalled until the request can be serviced. If a miss occurs on the data cache, the memory pipeline stalls, but the fetch and execute pipelines continue to flow, until another memory operation needs to be initiated.--

Rewrite the paragraph at page 56, line 1 as follows:

--Pseudocode ~~foe~~ for the procedures is listed below:--